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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,794	11/21/2003	Lorenzo Di Gregorio	068758.0146	3086

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Andreas Grubert
Baker Botts L.L.P.
One Shell Plaza
910 Louisiana
Houston, TX 77002

EXAMINER	
LAI, VINCENT	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 09/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,794	DI GREGORIO ET AL.	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *38-74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *38-74* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
9/27/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copies of the priority documents have been received.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 11/21/2003 was considered by the examiner.

Response to Amendment

3. Acknowledgment is made of the amendments to the title, specification and claims.

4. Objections to title and specification are withdrawn after considering amendments.

5. Claim objections and rejections are moot after claim cancellations

Claim Objections

6. Claim 46 is objected to because of the following informalities: Claim 46 is dependent on a claim that comes after itself. Appropriate correction is required.

Response to Arguments

7. [Examiner's Note: The reply filed on 13 July 2006 is not fully responsive to the prior Office Action because of the following omission(s) or matter(s): "The reply must present arguments pointing out the specific distinctions believed to render the claims, *including any newly presented claims*, patentable over any applied references (emphasis added)." Admitted newly presented claims 73 and 74 have no arguments in the reply but are explicitly made apparent that the claims are indeed newly presented claims. "*A general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the reference does not comply with the requirements of this section* (emphasis added)." See 37 CFR 1.111 (b). Examiner, will however, examine the newly presented claims].

8. Applicant's arguments with respect to claims 38-74 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 38-45, 47-55, and 57-74 are rejected under 35 U.S.C. 102(e) as being anticipated by Sturges et al (U.S. Patent # 7,047,399 B2), herein referred to as Sturges.

[Examiner's Note: Claims 1-37 have been cancelled by Applicant]

As per **claim 38**, Sturges discloses a device for controlling processing of data elements wherein threads are assigned to each data element and no more than one data element enters the device at one time (See column 7, lines 22-24: Such is the case in most processors. Instructions are fetched one at a time and nowhere does Sturges suggest more than one data element can enter any device at one time), comprising:

a first unit (See figure 10: One of the two fetchers) operable for storing context associated with corresponding threads, wherein the first unit is configured to fetch a first unit instruction (See figure 10: Both fetchers can fetch an instruction) and store the first unit instruction in a context associated with a thread assigned to an incoming data element (See figure 11: The state is saved in the state register), wherein the context contains context information indicative of a present state of the thread (See column 8, lines 14-16: A state indicator indicates context);

a second unit (See figure 10: One of the two fetchers) configured to fetch a second unit instruction, which succeeds a stipulated instruction in a sequence of instructions of a stipulated thread (See column 15, lines 37-39: If not branch is needed,

the fetchers swap (It is assumed "swop" is actually swap) roles, thus the first fetcher would fetch one instruction and the second would fetch the next); and

a third unit (See figure 10: Decode in the pipeline), configured to decode a selected instruction selected from the group consisting of the first unit instruction and the second unit instruction and generate a control signal for processing of the data element (See figure 11: The state is set after decoding).

As per **claim 39**, Sturges discloses wherein

the second unit instruction succeeds the stipulated instruction by one instruction (See column 15, lines 37-39: If not branch is needed, thus the first fetcher would fetch one instruction and the second would fetch the next. This means that the second unit would thus fetch the next instruction).

As per **claim 40**, Sturges discloses wherein

the second unit is configured to receive an increment of a count value (See column 9, lines 54-58: Count or offset value) and an identification value which designates a thread (See column 9, lines 54-58: Branch point), and

the second unit is configured to use the increment of the count value and the identification value to determine the second unit instruction (See column 9, lines 45-58: An offset value would mean an address would have to be computed).

As per **claim 41**, Sturges discloses wherein the first unit is configured to activate a new context that is associated with the thread assigned to the incoming data element if a preceding data element is assigned to another thread (See column 6, lines 26-28).

As per **claim 42**, Sturges discloses wherein

the first unit is configured to fetch (See figure 10: Has a fetcher), responsive to activating the new context (See column 6, lines 26-28), a first instruction of the incoming date element thread and transmit the first instruction to the third unit for decoding (See figure 10: Both fetchers send data to decoder); and

the first unit is configured to transmit an increment of the position that the instruction fetched by it assumes in the thread, to the second unit (See column 11, lines 39-41).

As per **claim 43**, Sturges discloses wherein

the second unit is configured to determine the instruction that succeeds the instruction fetched by the first unit in the thread (See column 11, lines 50-54).

As per **claim 44**, Sturges discloses wherein

the selected instruction is repeated for successive data elements until a stipulated condition is fulfilled (See column 10, lines 37-38).

As per **claim 45**, Sturges discloses wherein

the third unit is configured to cause repetition of the selected instruction by causing repetition of a control signal (See figure 10 and column 18, lines 48-51: Loops are done with the "set branch" and "do branch" blocks).

As per **claim 47**, Sturges discloses wherein

responsive to fulfillment of the stipulated condition, a stipulated instruction within a currently assigned thread is used for processing of a succeeding data element entering the device next if a thread assigned to the succeeding data element is the same as the currently assigned thread (See figure 10 and column 18, lines 48-51: This is true of loops).

As per **claim 48**, Sturges discloses wherein

the third unit is configured to determine the fulfillment of the stipulated condition (See figure 10: The third unit includes the execution pipeline and thus will be able to determine fulfillment).

As per **claim 49**, Sturges discloses wherein

the stipulated instruction is the second unit instruction fetched by the second unit (See figure 10: The second unit may be able to fetch the stipulated instruction).

As per **claim 50**, Sturges discloses further comprising:

a connection between the second unit and the third unit, via which the second unit instruction is transmitted to the third unit (See figure 10).

As per **claim 51**, Sturges discloses wherein

the second unit instruction fetched is transmitted to the first unit (See column 17, lines 15-16: Contents of fetchers can be transferred) and entered in a context therein (See column 6, lines 26-28).

As per **claim 52**, Sturges discloses wherein

the stipulated instruction is fetched by the first unit (See figure 10: Both fetchers can fetch an instruction) and transmitted to the third unit for decoding (See figure 10: Both fetchers send data to decoder).

As per **claim 53**, Sturges discloses wherein

the third unit, after fulfillment of the stipulated condition, transmits an instruction to the first unit indicative of which instruction is to be fetched (See figure 10: After decoding a target pointer is set).

As per **claim 54**, Sturges discloses further comprising

the stipulated condition comprises a condition selected from the group consisting of assertion of a signal controllable from outside of device (See column 12, lines 18-19), detection of a specific data element entering the device (See column 12, lines 24-27),

detection of a specific state of the currently assigned thread (See column 8, lines 14-16: A state indicator), and detection of a specific instruction to be processed (See figure 10: Instruction would be whatever is given to execution unit).

As per **claim 55**, Sturges discloses further comprising

a program memory including instructions for processing of the data elements (See column 7, lines 39-45: Instructions are fetched from memory) and information corresponding to at least one instruction indicative of to how many data elements the instruction is to be applied (The number of data elements involved with an instruction is inherent).

As per **claim 57**, Sturges discloses the limitations for reasons paralleling the reasons advanced above with respect to claim 38, as per admission by Applicants that claims are parallel.

As per **claims 58-72**, Sturges discloses the limitations for reasons similar to reasons discussed above in the rejections of claims 38-45 and 47-55.

As per **claims 73-74**, Sturges discloses the limitations for reasons similar to reasons discussed above in the rejections of claims 38-45 and 47-55. Being "sequentially adjacent" is similar to being "succeeds...by one," only it also included the

case where it is preceded by one, which is covered in the rejections when the first and the second units are switched.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sturges.

As per **claim 46**, Sturges teaches wherein the number of repetitions of the selected instruction is stipulated by a value (See column 10, lines 30-38: Stipulated by a value in the set instruction).

Sturges does not teach wherein the loop is a decrementing loop where the repetitions are interrupted when the value reaches zero.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Sturges to include decrementing loops since decrementing loops are well known in the art and Sturges already teaches loops in a general form.

11. Claim 56 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sturges in view of Shimazaki et al (U.S. Patent # 5,483,552), herein referred to as Shimazaki.

In **claim 56**, Sturges et al teaches the devices as claimed in claim 38 (See the 35 USC 102b rejection of claim 38).

Sturges does not teach a delay unit.

Shimazaki does teach a two series-connected delay units that delay the data element by one clock cycle each (See column 5, lines 42-45: There are two delay units connected in series and delays any amount of time, including one clock cycle).

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Sturges to include a delay unit because a delay unit allows for delaying the use of data and thus ensures that data is received is proper (or equalized) (See Shimazaki column 4, lines 26-30), since data propagation may be delayed due to numerous reasons well known to a person having ordinary skill in the art at the time of the invention. This improvement would lead to greater reliability and more likelihood that the prefetched data will be ready for use when it is needed.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
9/27/2006

vl
September 26, 2006